2024 9th International Symposium on Computer and Information Processing Technology (ISCIPT) | 979-8-3503-8840-4/24/$31.00 ©2024 IEEE | DOI: 10.1109/ISCIPT61983.2024.10672949

Design of signal conditioning circuit for sonar receiver with strong anti-interference ability

Peihong Wang[1,2,3,4], Jianjun Zhu[*,1,2,3,4], Yufei Zhai[2,3,4], Morgunov Yuri Nikolaevich[5], Baowei Chen[1,2,3,4], Smolenskii Egor[5]

[1] Sanya Nanhai Innovation and Development Base of Harbin Engineering University, Sanya, 572000, China

[2]National Key Laboratory of Underwater Acoustic Technology, Harbin Engineering University, Harbin 150001,China

[3]Key Laboratory of Marine Information Acquisition and Security(Harbin Engineering University),Ministry of Industry and Information Technology;Harbin 150001,China

[4]College of Underwater Acoustic Engineering, Harbin Engineering University, Harbin 150001, China

[5]Pacific Oceanological Institute of the Far Eastern Branch of the Russian Academy of Sciences, Vladivostok 690950, Russia

Corresponding Author: jianjun Zhu

Email: zhujianjun@hrbeu.edu.cn

***Abstract*—This paper mainly introduces a sonar receiver signal conditioning circuit, mainly including the front impedance matching circuit, two-stage differential filter amplifier circuit, variable gain amplifier circuit. Circuits at all levels in the design of the low noise program, the use of full differential circuit form, improve the receiving system noise resistance. Circuit using the appropriate combination of structure, optimization of PCB wiring, the design of the four-channel signal conditioning circuit PCB size of 4.1cm × 2.7cm. Finally, the circuit is physically tested, the results show that the design specifications in line with the requirements. Can effectively docking retrieved hydroacoustic target signal amplification, filtering, noise reduction and other conditioning.**

Keywords-Underwater acoustic; Signal conditioning circuit; Low noise; Front-stage impedance matching circuit; Differential filter amplifier circuit; Variable gain circuit

I. INTRODUCTION

Sonar is an important hydroacoustic device for detecting and recognizing underwater targets and for underwater acoustic communication and other applications [1]. The sonar receiver signal conditioning circuit amplifies and filters the analog signal output from the transducer, improves the signal-to-noise ratio of the system, and supports subsequent high-quality digital signal processing [2]. The sonar receiver signal conditioning circuit is an important part of the sonar system, which directly affects the performance of the entire sonar system. Anti-interference, anti-signal aliasing, is an important technical indicator of this type of circuit. The weak echo analog signal received by the sonar receiver is susceptible to external environmental noise and circuit noise interference, the existing technology in the sonar receiving system circuit scale, is not conducive to the high integration design of the circuit system and the miniaturization of the equipment, is not conducive to the subsequent development of high-quality digital signal processing, and it is gradually difficult to support the development of high-performance portable sonar system of the urgent needs[3]. Accordingly, this paper designs a sonar receiver signal conditioning circuit with small size and strong noise immunity.

II. MATERIALS AND METHODS

In this paper, a signal conditioning circuit with strong anti-interference capability is designed, constructed with rail-to-rail voltage feedback type amplifier, full differential amplifier, and analog-controlled variable gain amplifier (VGA) as the core devices, which can condition the small-amplitude analog signals output from the transducer, and output signals with high quantization-to-noise ratios (SQNR) to satisfy the requirements of precision analog-to-digital converters (ADCs), and it is applicable to the detection of sonar, navigation sonar, communication sonar and other sonar.

This design adopts a low-noise design scheme, which significantly improves the system's anti-interference capability by carefully optimizing the circuit topology, selecting low-noise components, appropriate types of filters, and using different devices to eliminate noise. When designing the filter, an analog bandpass filter with a flat passband and steep transition band in the desired frequency range is selected to effectively suppress noise interference. The noise performance of the whole system mainly depends on the fixed gain circuit of the preamplifier stage, which has low noise, and the whole system can obtain good low-noise performance. In order to make the noise of the whole system as small as possible, this design sets the gain of the preamplifier circuit to 0 dB. Meanwhile, RC passive filters are set at the connection of the circuits of each stage, the input and output of the signal to further eliminate noise. At the same time, the selection of magnetic beads (high-frequency filter), filtering power supply high-frequency noise, weakening electromagnetic interference. In the PCB wiring, the principle of differential distribution lines to reduce the noise of the input signal. All circuits use differential circuitry, which can effectively suppress electromagnetic interference, timing positioning accuracy and other characteristics.

At the same time, this design adopts an innovative circuit structure design ideas, greatly streamlining the circuit structure and scale, and improve the circuit efficiency and performance using the THS4561 full differential amplifier will be a combination of fixed gain circuits and band-pass filtering circuits, while realizing the two functions of filtering and fixed-gain amplification. It effectively reduces the cost while simplifying the circuit structure.

III. SIGNAL CONDITIONING CIRCUIT DESIGN

The sonar receiver typically consists of signal conditioning circuitry, AD conversion circuitry, gain control circuitry (DAC), power supply circuitry, and other components [4]. Its operational block diagram is illustrated in Figure 1.

The design indicators of the receiver of this system are as follows: operating center frequency 140kHz, bandwidth 60kHz; gain range 0dB-80dB; maximum working distance 100m, minimum working distance 2m.

The signal conditioning circuit is mainly used to condition, amplify and filter the electrical signals received through the transducer to facilitate ADC acquisition, improve the system signal-to-noise ratio, and resist aliasing [5]. It mainly includes front-stage impedance matching circuit, differential filter amplifier circuit, and variable gain amplifier circuit. as shown in Figure 2.

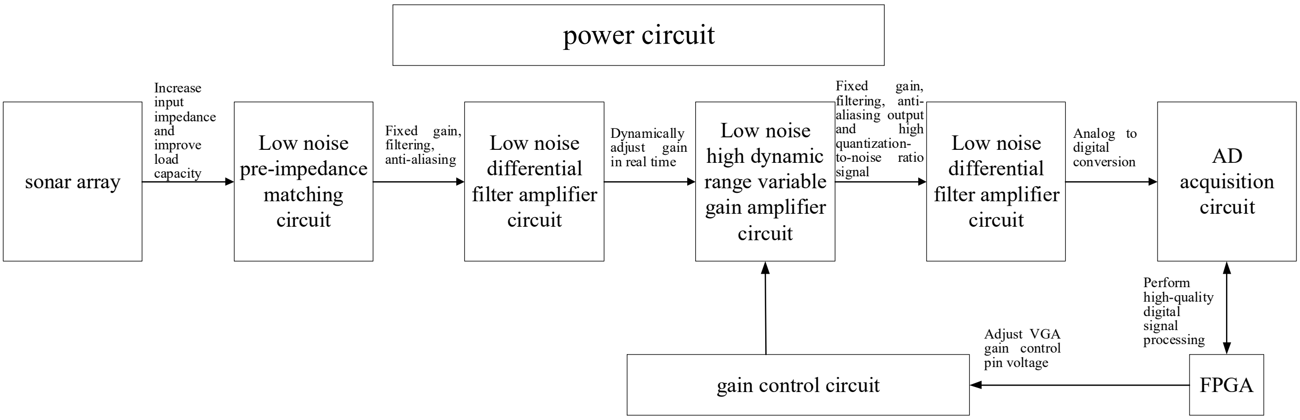


Figure 1 Block diagram of sonar receiving system

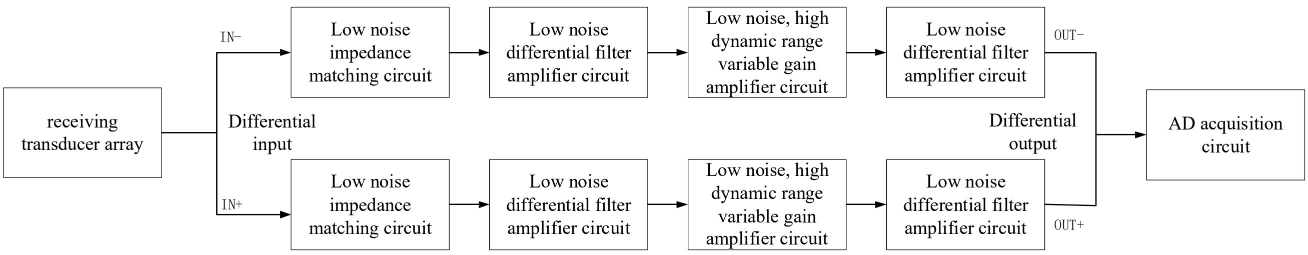


Figure 2 Receiver signal conditioning circuit

The signal conditioning circuits designed in this article all adopt the form of differential circuits. Compared with single-ended circuits, they have the characteristics of strong anti-interference ability, effective suppression of electromagnetic interference, and accurate timing positioning. When noise enters both ends of the differential circuit, since the receiving end processes the difference between the two signals, the circuit cancels most of the noise to a large extent [6]. At the same time, because the polarity of the signals at the two ends of the differential circuit is opposite, the external radiation Electromagnetic interference can cancel each other out. The switching change of the differential signal is located at the intersection of the two signals and is less affected by process and temperature, which can effectively reduce timing errors.

A. Low noise impedance matching circuit design

The impedance matching circuit of the pre-stage of the signal conditioning circuit is related to the noise performance of the receiver circuit. If the noise of this stage is low, the entire receiving system can obtain good low-noise performance. In order to make the noise of the entire system as small as possible, the impedance matching circuit gain can be set to 0dB. On the premise of considering the noise of the impedance matching circuit, the load capacity and common mode rejection ratio of the circuit must also be improved. Using a differential amplifier circuit can significantly improve the anti-interference ability, increase the circuit input impedance and load capacity [7].

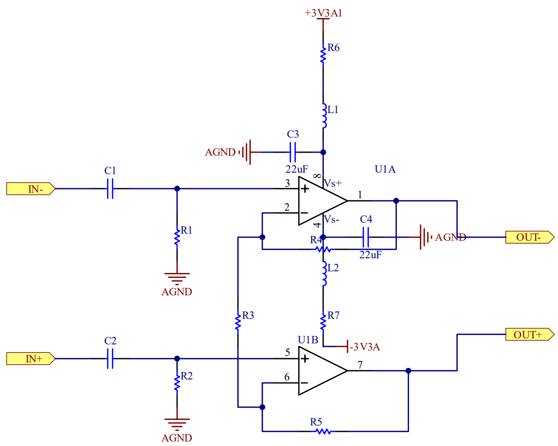


Figure 3 Schematic diagram of low-noise impedance matching circuit

The ADA4807-2 is a low-power, low-noise rail-to-rail voltage feedback amplifier with input noise of only 3.1nV/ √ Hz and 0.7pA/ √ Hz, and quiescent supply current of less than 1mA, delivering ultra-high performance. To this end, the fixed gain circuit uses a differential amplifier circuit constructed from ADA4807-2. The schematic is shown in Figure 3.

According to the actual design index requirements, the circuit gain can be changed by adjusting the resistance values of R_3R_3、R_4、R_5. The gain calculation formula of the circuit is

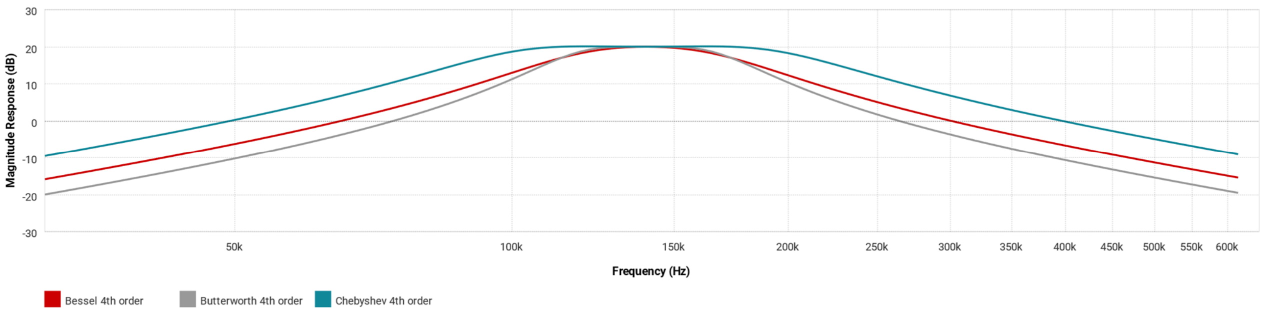
$$G = 1 + \left(\frac{R_4 + R_5}{R_3} \right). \tag{1}$$

The RC filter in the circuit above is mainly used to filter out low-frequency noise at the signal input end. Magnetic bead L1 is a high-frequency filter device, used in this circuit to filter high-frequency noise from the power supply and weaken electromagnetic interference.

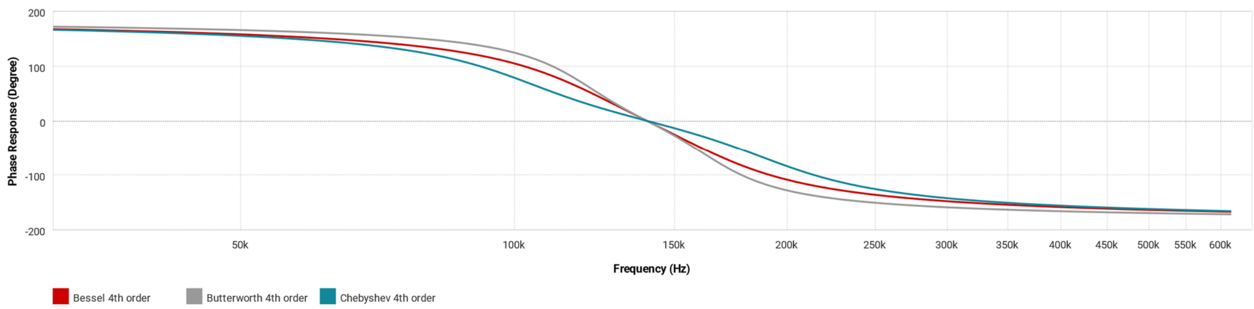
B. Low noise differential filter amplifier circuit

In addition to the echo signal of the detection target, the signal received by the receiver also contains many noise components, such as marine environment noise, ship noise, etc [8]. In order to effectively eliminate noise interference, the filter circuit must be designed reasonably. Good filtering performance can effectively reduce the sampling rate of the ADC and reduce the occurrence of signal aliasing, reducing the design and development difficulty of the digital signal processing platform.

Figure 4 shows the amplitude-frequency characteristics and phase-frequency characteristics of a fourth-order bandpass filter with a center frequency of 140kHz, a bandwidth of 60kHz, and a gain of 20dB. It can be seen that the amplitude-frequency characteristics of the Chebyshev filter fluctuate within the passband. , the Bessel type filter is not stable enough in the passband, and the Butterworth filter has a flat passband and good stopband attenuation, and the phase-frequency characteristics are also close to linear in the operating frequency range. Therefore, this design finally chooses the fourth-order bandpass Butterworth filter to design the bandpass filter circuit.



(a)Amplitude-frequency characteristics



(b)Phase-frequency characteristics

Figure 4 Comparison of response characteristics of three typical filters

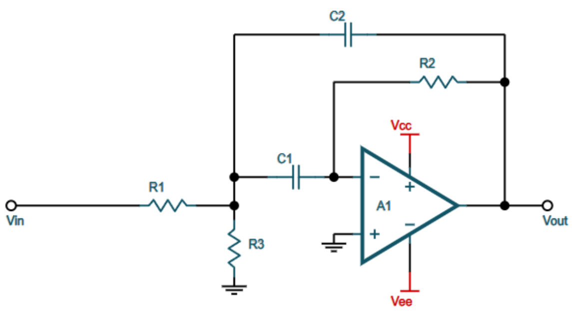


Figure 5 Infinite gain multi-channel negative feedback bandpass filter topology

The filter circuit has two topologies: voltage-controlled voltage source type and infinite gain multi-channel negative feedback type. Among them, the infinite gain multi-channel negative feedback topology has lower sensitivity to components and requires fewer components than the voltage-controlled voltage source circuit. Therefore, the infinite gain multi-channel negative feedback topology is selected for the design, as shown in Figure 5 shown.

The transfer function of the infinite gain multi-channel negative feedback bandpass filter is

$$H_{BP}(S)=\frac{-\frac{1}{R_1C_1}S}{S^2+\frac{C_1+C_2}{R_3C_1C_2}S+\frac{R_1+R_2}{R_1R_2R_3C_1C_2}}. \quad (2)$$

Comparing the transfer function with the standard function we get

$$Q=\frac{w_0}{B}$$
$$w_0=\frac{1}{\sqrt{(R_1//R_2)R_3C_1C_2}} \quad (3)$$
$$G=\frac{R_3}{R_1\left(1+\frac{C_1}{C_2}\right)}$$

In the actual debugging of the circuit, C can be adjusted first to obtain the specified w0. Then adjust R_2 to obtain the specified Q. THS4561 is a low-power, 60MHz, wide power supply voltage range fully differential amplifier, which can be used to form a differential fourth-order band-pass filter. The gain can also be set to reduce the scale of the entire conditioning circuit. Two THS4561s are used to form a fourth-order bandpass filter with a center frequency of 140kHz, a bandwidth of 60kHz, and a gain of 20dB. This level of circuit can combine a fixed gain circuit and a band-pass filter circuit to achieve amplification and filtering functions at the same time, which can reduce the circuit volume. An RC filter circuit can be added to the output of each stage of the circuit to further eliminate the impact of noise interference.

In order to ensure the amplitude consistency and phase consistency of the receiver channel, selecting high-precision resistor-capacitor components with an accuracy of 0.1% can meet the design requirements.

C. Low noise variable gain circuit design

There are three main control types of variable gain amplifier circuits, namely resistance control type, voltage control type and coding control type. Among them, the resistance control type and the code control type are only suitable for receivers with few required gain levels. The voltage control type can continuously control the circuit gain by adjusting the voltage of the VGA chip gain control pin. Therefore, this design uses a voltage-controlled variable gain amplifier circuit.

The AD8338 chip is a variable gain amplifier for fully differential signal paths and features low power consumption, low noise, small size, and high precision gain control in the 18MHz band. By adjusting the voltage 0.1V-1.1V on the gain pin, 0dB-80dB linear gain control is realized, which can meet the requirements of the system gain range index.

The relationship between the control gain value and Vgain is shown in Figure 6. There are two control modes: positive gradient control mode and negative gradient control mode. In order to facilitate PCB wiring, this design uses the negative gradient control mode. Adjusting the Vgain voltage of the VBAT pin (0.1V-1.1V) can achieve linear dynamic control of the gain.

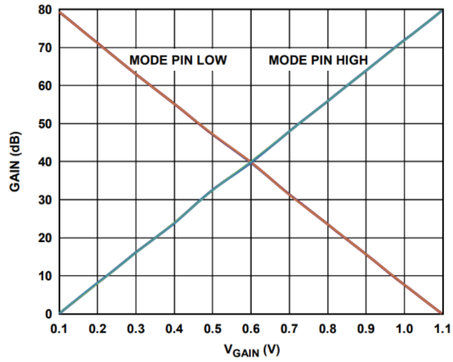


Figure 6 Relationship between AD8338 gain and Vgain

The AD8338 can use the internal reference voltage for all signal processing and requires no external configuration. For applications requiring DC coupling to the ADC, a differential amplifier must be used. The maximum output voltage of AD8338 is about 1V, and the reference voltage of the AD chip is 4.096V. Therefore, a differential amplifier with a 12dB gain needs to be connected after the AD8338. The THS4561 fully differential amplifier provides a simple interface between differential outputs to meet the needs of precision analog-to-digital conversion. The buffer circuit before the ADC can be designed as a second-order differential filter amplifier circuit with 12dB gain, which can further filter noise and eliminate noise interference. The schematic diagram is shown in Figure 7.

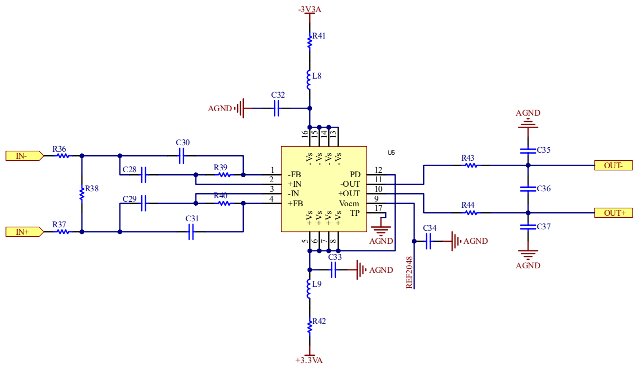


Figure 7 Differential filter amplifier circuit

Connect resistors R_{28} and R_{29} in series to the INMD and INPD pins, and negative gain can be achieved by adjusting the resistance values of R_{28} and R_{29}. The system gain requirement is 0dB-80dB. The fixed gain of the AD8338 front stage is 20dB, and the rear stage is connected to a differential amplifier with a gain of 12dB. Therefore, the gain range of the AD8338 needs to be configured as (-32dB-48dB). The specific resistance size can be calculated by the following formula.

$$Gain(dB)=(1.1-V_{GAIN})\times 80+20\log\left(\frac{9.5k}{R_{IN}}\right)-26. \quad (4)$$

The schematic diagram of the designed variable gain circuit is shown in Figure 8. An RC filter circuit is added to the input and output ends of the signal to further suppress circuit noise.

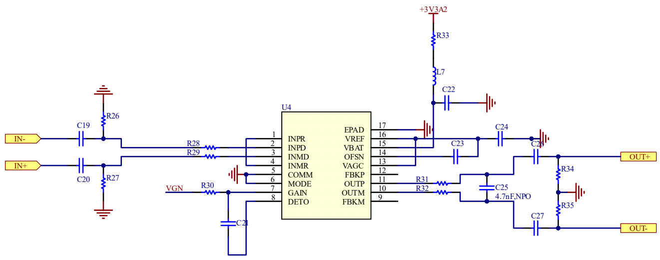


Figure 8 Variable gain circuit schematic diagram

IV. Signal Conditioning Circuit Testing

After checking that there are no errors, the circuit PCB is drawn using Altium Designer to reduce the size of the circuit and improve the performance by means of shortest path, differential matching, and interlayer wiring. The PCB size of the four-channel sonar signal conditioning circuit is 4.1cm×2.7cm, and the PCB size layout is shown in Figure 9.

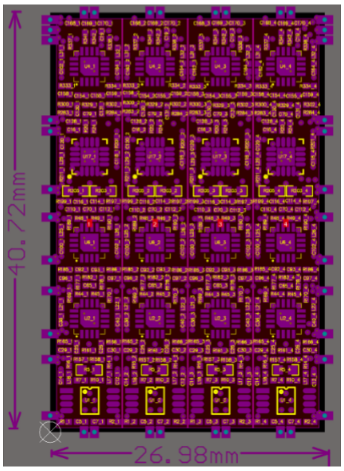


Figure 9 PCB Dimension Layout

The actual circuit was tested using a signal source, oscilloscope, multimeter, etc., as shown in figure 10.

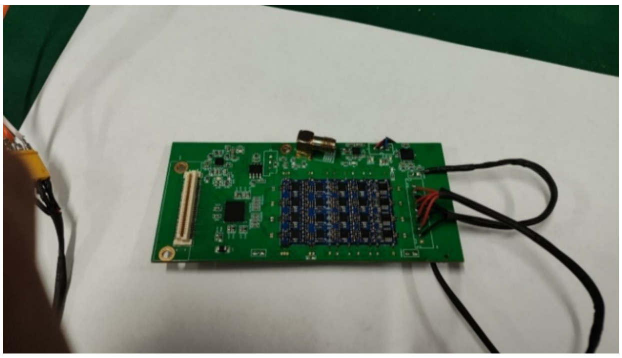


Figure 10 Actual circuit test environment diagram

Test the center frequency and bandwidth of the filter, and perform a frequency sweep test as shown in Figure 11.

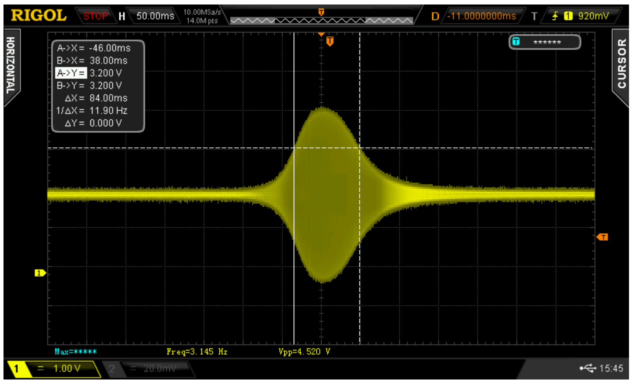


Figure 11 Frequency sweep test results of differential filter amplifier circuit

The frequency sweep bandwidth is 1kHz to 500kHz, and the frequency sweep time is 700ms. Then the bandwidth of the receiver is $\Delta x/(700ms)\times 499kHz = 59.88kHz$ .After unfolding the signal, the center frequency was measured to be 140.6kHz. It is consistent with the design specifications and within the normal error range.

Variable gain circuit test: By adjusting the gain voltage of the AD8338 VBAT pin and measuring the actual output voltage value, calculate the deviation between the actual amplification factor and the theoretical amplification factor, as shown in Table 1 (retaining two decimal places).

Table 1 Variable gain circuit amplification test data table

VBAT pin voltage (V)	Theoretical gain(dB)	Theoretical magnification	Input signal amplitude (mV)	Theoretical output signal amplitude (mV)	Actual output signal amplitude (mV)	Difference (mV)
0.8	24	15.85	10.27	162.77	156.60	6.17
0.7	32	39.81	10.00	398.11	400.00	1.89
0.85	20	10.00	10.00	100.00	108.00	8.00
0.9	16	6.31	20.00	126.19	134.00	7.81
1	8	2.51	108.00	271.28	272.00	0.72
1.1	0	1.00	228.00	228.00	224.00	4.00

The average differences are all within 8mV. Taking into account the influence of signal noise and instrument errors during testing, the errors are within the allowable range and can be used normally.

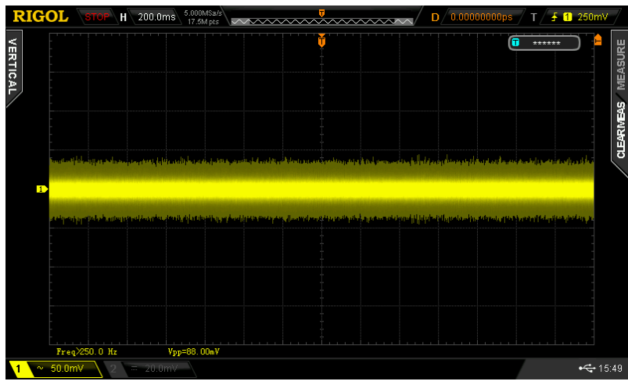


Figure 12 Equivalent noise test chart

Sonar receiver equivalent input noise test: short-connect the in-phase input end of the receiver and the inverting input end, and adjust the voltage of the VBAT pin of the AD8338 to 0.1V, so as to achieve variable gain of 48dB and fixed gain of 32dB, so as to form a total circuit gain of 80dB. Connect the oscilloscope pen grounding clip to GND, and connect the probe end to the output test point of the amplitude-modulation circuit. The measured output noise RMS value is 88mV, as shown in Figure 12.

Based on this, the equivalent input noise is calculated as

$$V_{noise} = \frac{88\times10^{3}}{10^{80/20}} = 8.8\mu V \tag{5}$$

V. CONCLUSIONS

In this paper, the sonar receiver signal conditioning circuit is designed and verified. Each stage of the circuit adopts the differential form, which can significantly improve the noise immunity of the system. At the same time, the THS4561 full differential amplifier chip is selected to form a differential filter amplifier circuit, the fixed gain circuit and bandpass filter circuit are combined together to realize the amplification and filtering functions at the same time, which simplifies the differential circuit form and hardware scale, and the PCB size of the four-channel receiver signal conditioning circuit designed is 4.1cm×2.7cm. The circuit adopts modular design, so that when facing different demands, the receiving system only needs to replace the signal conditioning circuit, and at the same time, the circuit is simple to debug, and only needs to replace some capacitance resistance to change the signal conditioning circuit indexes, which can satisfy different system demands, and save the cost of sonar hardware. The signal conditioning circuit of sonar receiver designed in this paper is characterized by low noise, low power consumption, clear principle, etc. The design and verification method is also of reference value for the design of other receiving system circuits.

ACKNOWLEDGMENT

Thanks to Shoumeng Sheng, Zhanxi Wu and Doctor Xinbao Meng for their contributions in the technical research process. This work was supported by the Hainan Provincial Natural Science Foundation of China [grant numbers 421CXTD442], the National Natural Science Foundation of China [grant numbers 42176188] and the Stable Supporting Fund of Acoustic Science and Technology Laboratory [numbers JCKYS2024604 SSJS004].

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